

# **SPECIFICATION**

Title of the Invention :

**PILOT SIGNAL RECEPTION METHOD AND RECEIVER**

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## PILOT SIGNAL RECEPTION METHOD AND RECEIVER

## BACKGROUND OF THE INVENTION

## 5 Field of the Invention

The present invention relates to a pilot signal reception method and receiver.

## Description of the Related Art

10 In a CDMA communication, a pilot signal is used to acquire synchronization in a mobile station, create a delay profile and correct frequencies in a mobile station, and adjust reception timings in a mobile station, etc. This pilot signal is sent from a base station.

15 An IS-95-compliant communication system is provided with a dedicated pilot channel 100 as shown in FIG.12A.

Furthermore, in a new standard W-CDMA system, a dedicated pilot channel 101 is provided in addition to  
20 a channel with pilot signals (PL) inserted at predetermined intervals.

That a dedicated pilot signal channel exists means that pilot signals are output from the transmitting side all the time.

25 A concrete pilot channel (100 and 101) format example is shown in FIG.12C.

What is shown in the upper part of FIG.12C is an example of a pilot signal subjected to data modulation

(format example 1).

That is, in the case of format example 1, the pilot channel is configured by slots made up of a set of several to a few tens of symbols, which are information units spread using a specified number of spreading code chips.

Furthermore, in the example shown in the lower part of FIG.12C (format example 2), no data modulation is applied to the pilot channel. For example, since a common pilot channel is commonly used by base stations, the common pilot channel need not be subjected to data (symbol) modulation and such a format without data (symbol) modulation (that is, format with no symbol concept) is also accepted.

Here, reception of a spread/modulated pilot channel will be considered.

When receiving pilot signals, it is desirable to intermittently receive the pilot signals rather than receiving the pilot signals all the time and thereby reduce the amount of pilot data in order to alleviate load on a circuit carrying out signal processing such as a DSP and reduce the amount of pilot data.

The inventor of the present invention has studied a method of performing despreading processing and then demodulation on a predetermined number of known symbols in slots at predetermined timings as shown in FIG.14.

As a result, it has been discovered that reception according to this method provides cyclic and burst-like demodulation of pilot symbols, and therefore can provide

reception with low reliability at most when the intensity of the signal is reduced due to cyclic fading or burst-like fading.

That is, as shown in the lower part of FIG.14, in the case where a reception timing (reception segment) of a pilot signal coincides with a valley of cyclic variation of the intensity of the reception signal, an S/N (reception quality) with respect to reception of the pilot signal deteriorates. Therefore, the reliability of data in the reception segment is also reduced.

The present invention has been implemented focusing on such investigation results and it is an object of the present invention to attain reception of pilot signals with high reliability by reducing adverse influences of fading.

#### SUMMARY OF THE INVENTION

The present invention performs reception of pilot symbols irregularly.

That is, the present invention performs irregular reception processing by randomizing reception timings or changing reception timings by adapting reception timings to reception situations as appropriate. This makes the system less susceptible to cyclic or burst-like fading.

In the case where a spread signal including a dedicated pilot signal channel is received, the

reception method of the present invention divides the reception signal into two systems. The signal on one system is subjected to normal despreading to demodulate data other than pilot signals. The signal on the other  
5 system is subjected to irregular despreading to demodulate pilot signals.

An aspect of the pilot signal reception method of the present invention generates completely random timings using random numbers, etc.

10 Another aspect of the pilot signal reception method of the present invention despreads signals at timings other than the timing of despreading in the previous time segment.

Another aspect of the pilot signal reception method  
15 of the present invention measures the signal intensity of symbols after despreading and changes the despreading timing in such a way as to avoid reception at a timing corresponding to valleys of fading.

Another aspect of the pilot signal reception method  
20 of the present invention predetermines (irregularly) the positions (timing) at which pilot symbols are placed between a transmission apparatus and reception apparatus on a channel where symbols other than the pilot symbols are also placed. Then, despreading is carried out using  
25 a random timing generator common to the transmitting side and receiving side.

An aspect of a CDMA receiver of the present invention comprises an A/D converter, despreading

circuit, random timing generation circuit, reception control circuit and phase/signal intensity detection circuit. This configuration makes reception timings irregular, allowing the system to perform reception less susceptible to cyclic, burst-like fading.

Another aspect of the CDMA receiver of the present invention comprises a despread timing determination circuit and a despread timing retention circuit that retains timings generated by the despread timing determination circuit and the despread timing generation circuit changes reception timings based on past despread timings retained by the despread timing retention circuit. This configuration allows despread to be performed at a timing different from the immediately preceding reception timing. Thus, this configuration allows the system to perform reception less susceptible to cyclic fading.

Furthermore, another aspect of the CDMA receiver of the present invention adopts a configuration that returns the output of the despread circuit to the despread timing determination circuit. This configuration makes it possible to determine despread timings based on the intensity of the despread signal and perform reception that matches the reception situation.

Furthermore, another aspect of the CDMA receiver of the present invention adopts a configuration comprising a despread chip number determination

circuit and allowing the output of the despread-  
ing circuit to be input to the despread-  
ing chip number  
determination circuit. This configuration allows a  
channel not subjected to data modulation to be

5 demodulated by despread-  
ing by an arbitrary number of  
chips from a certain chip. This enhances the flexibility  
of despread-  
ing timings. It is also possible to  
adaptively change the number of chips to be despread  
according to the situation of the propagation path.

10 Another aspect of the present invention allows both  
the transmission apparatus and reception apparatus to  
generate transmission timings and reception timings  
using a common random generation circuit.

15 BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects and features of the  
invention will appear more fully hereinafter from a  
consideration of the following description taken in  
20 connection with the accompanying drawing wherein one  
example is illustrated by way of example, in which;

FIG.1 is a block diagram showing a configuration  
example of a demodulation section of a CDMA receiver of  
the present invention;

25 FIG.2 is a block diagram showing a specific  
configuration example of the despread-  
ing circuit shown  
in FIG.1;

FIG.3 is a flow diagram showing characteristic

operations of the despreading circuit shown in FIG.2;

FIG.4 is a block diagram showing another configuration example of the demodulation section of the CDMA receiver of the present invention;

5        FIG.5 is a diagram showing an example of despreading timing in the demodulation section of the CDMA receiver in FIG.4;

FIG.6 is a block diagram showing another configuration example of the demodulation section of the CDMA receiver of the present invention;

FIG.7 is a diagram showing an example of despreading timing in the demodulation section shown in FIG.6;

FIG.8 is a block diagram showing another configuration example of the demodulation section of the receiver of the present invention;

FIG.9 is a block diagram showing a configuration example of the apparatus on the transmitting side to implement another example of the pilot signal reception method of the present invention;

20        FIG.10 is a block diagram showing a configuration example of the apparatus on the receiving side to implement another example of the pilot signal reception method of the present invention;

FIG.11 is a block diagram showing a specific configuration example of the despreading circuit shown in FIG.10;

FIG.12A is a drawing to explain an example of communication method using pilot channels;



FIG.12B is a drawing to explain another example of communication method using pilot channels;

FIG.12C is a drawing showing a slot format example of a CDMA communication system;

5        FIG.13 is a drawing to explain an example of pilot signal reception method of the present invention;

FIG.14 is a drawing to explain the pilot signal reception method in a comparison example studied by the inventor of the present invention prior to the present invention; and  
10

FIG.15 is a drawing showing a signal format example used in the communication system explained in FIG.9, FIG.10 and FIG.11.

15                                DETAILED DESCRIPTION OF THE  
                                 PREFERRED EMBODIMENTS

With reference now to the attached drawings, embodiments of the present invention will be explained  
20 in detail below.

(Embodiment 1)

FIG.1 is a block diagram showing a main configuration of a CDMA receiver of the present  
25 invention.

As shown in the figure, this CDMA receiver is provided with A/D conversion circuit 1, despreading circuit 2, random timing (irregular timing)

determination circuit 3, reception control circuit 4 and phase/signal intensity detection circuit 5.

In order to perform coherent detection or correct the frequency of a reference clock in a receiver, it is  
5 necessary to determine phase variations in reception symbols.

To determine phase variations in reception symbols, it is necessary to determine variations in the intensity of symbol signals. For this reason, this embodiment is  
10 provided with phase/signal intensity detection circuit 5.

Synchronization acquisition, creation of a delay profile, correction of the frequency of a reference clock and adjustment of reception timings, etc. are carried  
15 out using the signal intensity of pilot symbols (pilot signals) detected in this phase/signal intensity detection circuit 5.

This embodiment makes reception timings of pilot symbols irregular using random timing determination  
20 circuit 3. This makes the system less susceptible to fading during reception of pilot signals.

When cyclic and intermittent pilot signals as shown in FIG.14 are received, the time period during which the intensity of the reception signal is lowered due to  
25 fading may coincide with the time period during which pilot signals are received. In this case, reception continues with low signal intensity all the time unless the fading cycle is shifted, which deteriorates the S/N

ratio and deteriorates reliability of reception.

Thus, reception timing information is generated by random timing generation circuit 3, which produces arbitrary timings not cyclically but randomly and  
5 reception control circuit 4 controls operation of despread-  
ing circuit 2 based on the reception timing information.

If pilot signals are received at random timings, the risk of directly receiving influences of the  
10 reduction in the reception intensity due to fading is reduced all the more because the reception timings are distributed. Thus, the average S/N ratio of the reception signal improves, making it possible to receive signals with high reliability. Despread-  
15 ing circuit 2 outputs a demodulated signal and transmits the demodulated signal to phase/signal intensity detection circuit 5.

Here, the term "random" is not limited to disorder in a strictly mathematical sense using a random numbers  
20 table, etc.

"Random" is used as a term that broadly means what is generally called "pseudo-random" or states which can be proven independent of each other without regularities between past, current and future states.

25 More specifically, the term "random" has also connotations "non-cyclic" or "not fixed" (that is, not regular). This specification expresses "irregular" including all these connotations.

A random signal can be generated using, for example, a random number generation circuit, a code generation circuit using predetermined functions. Moreover, it is also possible to randomize reception timings in a pseudo-form by registering multiple patterns about reception timings beforehand (patterns are mutually independent) and selecting one of these patterns according to the reception situation.

FIG.13 shows examples of reception at random timings.

In the reception example shown in the upper part of FIG.13, despreading is performed at irregular timings on a spread/modulated pilot channel (a concept of slot exists). In the figure, symbols to be despread are hatched.

On the other hand, the reception example shown in the lower part of FIG.13 is a case where a common pilot channel (without a concept of slot) without data modulation is received. In this case, it is possible to despread an arbitrary number of chips from a chip at a random position.

At the bottom of FIG.13 is an illustration showing how the intensity of the reception signal fluctuates. As is shown in the figure, the intensity of the reception signal fluctuates cyclically under the influence of fading.

On the other hand, reception timings of pilot signals are randomized. Therefore, the system is less

susceptible to fading and the average S/N of the reception signal improves.

Thus, randomizing reception timings prevents the intensity of the reception signal from extremely  
5 reducing under the influence of fading valleys even if the intensity of the reception signal cyclically fluctuates.

FIG.14 shows a comparison example where, for example, known symbol patterns are concentrated at  
10 predetermined locations in a slot and a predetermined number of symbols are received during a predetermined time period in the slot. In this case, when the reception segment coincides with the cycle of fading, the S/N of the reception signal will deteriorate extremely.

15 Thus, according to the CDMA receiver of this embodiment, it is possible to reduce the probability that reception timings of pilot signals will coincide with the period during which the intensity of the signal is lowered due to fading, making it possible to receive  
20 pilot signals with high reliability.

FIG.2 shows a concrete example of the circuit configuration of the despreading circuit 2.

Despreading circuit 2 applies despreading to a quadri-phase shift keying (QPSK) signal input. The  
25 signal input includes a dedicated pilot signal channel and other channels.

Despreading circuit 2 is provided with circuit 25 for despreading data other than pilot signals and circuit



That is, both circuits have I code generators 17 and 19, Q code generators 18 and 20, multipliers 10a to 10d and 14a to 14d, integrators 11a to 11d and 15a to 15d and comparators 12a, 12b, 16a and 16b, respectively.

15           FIG.3 shows main operations of despreading circuit  
2 shown in FIG.2.

That is, a spread/modulated signal including a dedicated pilot signal channel is received first (step 30). Here, the dedicated pilot signal channel is modulated by a specific (independent) spreading code. Channels other than the dedicated pilot signal channel are spread by different spreading codes.

Then, the reception signal is divided into two systems (step 31).

25           Then, the one system of the reception signal is subjected to desreading using a spreading code specific (independent) to the pilot signals at irregular timings and the other system of the reception signal is subjected

# 1. Introduction

to normal despreading using a different spreading code (step 32). Here, "irregular timing" includes non-cyclic timing, timing different from past timings, timing that varies according to the reception condition, 5 totally random timing determined by a random signal generator using random numbers, etc.

Despreading circuit 2 in FIG.2 divides the reception signal into two systems and performs processing on both systems simultaneously, which 10 achieves high processing efficiency.

Furthermore, despreading circuit 2 performs despreading on the dedicated pilot channel, which is sent from the transmitting side all the time, using a spreading code specific to the pilot channel. Thus, 15 there is no need to be aware of demodulation of other data. Thus, there are no restrictions on determining reception timings and it is possible to freely randomize reception timings.

Furthermore, the circuit in FIG.2 eliminates the 20 need for complicated switching operations of the switch to differentiate the pilot signals from other data, eliminates the need for complicated timing control and facilitates construction of the circuit.

25 (Embodiment 2)

FIG.4 shows another configuration example of the demodulation section of the receiver.

In this embodiment, a symbol reception timing in

a preceding slot is stored. Then, when a symbol reception timing in the next slot is determined, the stored timing or a predetermined period including this timing is designated as a selection prohibition period.

5 Then, symbol reception timings for the next slot are randomly determined.

First, a reception signal is quantized by A/D converter 51 and input to despreading circuit 52.

Despreading timing determination circuit 53  
10 generates reception timing information. The timing information is given to reception control circuit 55 and at the same time stored in memory 54.

The timing information immediately before being stored in memory 54 is returned to timing determination  
15 circuit 53.

When the timing determination circuit determines the next reception timing, the stored timing or a period close to this timing is designated as a reception prohibition period. Then, the next reception timing is  
20 randomly determined for other periods except the reception prohibition period.

Reception control circuit 55 controls operation of despreading circuit 52 based on the timing information. Despreading circuit 52 outputs a demodulated signal and  
25 transmits the demodulated signal to phase/signal intensity detection means 56.

FIG.5 shows an example of pilot signal reception timing.



In reception example 1 in FIG.5, the symbol currently being received ST1 (time  $t_1$  to  $t_2$ ) is assumed to correspond to a period during which the signal intensity of cyclic fading is low. That is, during reception of the next pilot signal, symbol ST1 is excluded from the symbol to be despread. Then, symbols to be received are randomly selected from among symbols other than symbol ST1.

In reception example 2 in FIG.5, the period ( $t_1$  to  $t_4$ ) including symbols before and after symbol ST1, which is currently being received, is designated as a period not to be despread during reception of the next pilot signal.

That is, a predetermined number of symbols including the symbol are excluded from the symbols to be received. Then, reception symbols are randomly selected from among other symbols.

In this way, in this embodiment, symbol reception in the next slot is determined in such a way as to exclude a symbol reception timing in one slot. This makes it possible to receive pilot signals resistant to cyclic and burst-like fading.

(Embodiment 3)

FIG.6 shows a configuration of the receiver of this embodiment.

In this embodiment, despreadings timings are adaptively changed based on the reception intensity of

a demodulated signal after desreading.

FIG.6 shows a main configuration of the receiver of this embodiment.

The output signal of desreading circuit 102 is fed  
5 back to desreading timing determination circuit 103 as a monitor signal.

Desreading timing determination circuit 103 measures the signal intensity of the demodulated signal over a plurality of slots.

10 When, the intensity of the reception signal is reduced (that is, reception reliability is lowered) under the influence of cyclic fading seen from the overall demodulation result of a plurality of slots, the period during which the reception intensity is low is  
15 designated as a reception prohibition period.

FIG.7 shows a reception example.

There is no problem if sufficient intensity of the demodulated signal is obtained as a result of desreading symbols in the current slot, and the next desreading  
20 can be performed at the same timing as the current one.

On the other hand, when the level of the demodulated signal jitters cyclically as in Example 1 of the intensity of the reception signal shown in the lower part of FIG.7, this can be considered as a reflection of fading  
25 with an extremely short frequency.

Thus, for symbol desreading in the next slot, symbol ST2 adjacent to the prohibited symbol ST1 is selected as the symbol to be received as shown in Example

1 of the next slot. That is, the reception timing is slightly delayed.

On the other hand, when the level of the demodulated signal fluctuates as in Example 2 of the intensity of the reception signal shown at the bottom of FIG.7, it can be considered that a temporary (burst-like) drop of the signal intensity spanning over a plurality of symbols is produced in the reception signal.

In this case, a certain period (time  $t_0$  to  $t_3$ ) including symbols ST0 and ST2 before and after the prohibited symbol ST1 as shown in Example 2 of the next slot is designated as a period not to be despread. Then, despread symbols are randomly selected from symbols outside the period and the despread timing (reception timing) is determined.

Based on the despread timing information determined in this way, reception control circuit 104 in FIG.6 controls operation of despread circuit 102. Despread circuit 102 outputs the demodulated signal.

Thus, this embodiment adaptively changes despread timings while measuring the reliability of the demodulated signal. This can make reception timings irregular (randomization) based on the actual reception situation. This makes it possible to receive fading-resistant pilot signals.

(Embodiment 4)

FIG.8 shows a configuration of the demodulation

section of the CDMA receiver of this embodiment.

In this embodiment, pilot signals are not subjected to data (symbol) modulation. That is, pilot channels have no concept of slot. Thus, it is possible to freely  
5 determine the reception segment of pilot signals.

That is, if the timing of a spreading code coincides with that of a reception signal, a correct despreading result can be obtained irrespective of which chip despreading is started with or up to which chip  
10 despreading is performed.

This embodiment is provided with despreading timing determination circuit 303 and despreading chip number determination circuit 304 and these circuits are received a demodulated signal output from despreading  
15 circuit 302.

Despreading timing determination circuit 303 determines the chip with which despreading is started at fixed intervals. The timing determination method in the despreading timing determination circuit is the same  
20 as the method explained in Embodiment 3, for example. The despreading chip number determination circuit determines the number of chips to be despread at fixed intervals.

Despreading chip number determination circuit 304  
25 analyzes the past reception situations and determines a carrier frequency error and a chip rate error.

When the carrier frequency error increases, phase rotation at symbol points also increases. For example,

when there is a large shift in the carrier frequency, if the number of chips to be despread is increased, the phase at the symbol point gradually rotates, which may prevent in-phase cumulative additions. Therefore, when  
5 the carrier frequency error is large, it is necessary to reduce the number of chips to be despread.

Furthermore, when the chip rate shift is large, increasing the number of chips to be despread is not so meaningful. Therefore, it is necessary to reduce the  
10 number of chips to be despread and carry out tracking operation whenever necessary.

The determined despreding timing and the signal indicating the number of chips to be despread are given to reception control circuit 305.

15 Reception control circuit 305 controls operation of despreding circuit 302. Furthermore, despreding circuit 302 outputs a demodulated signal and this demodulated signal is given to phase/signal intensity detecting means 306.

20

(Embodiment 5)

In this embodiment, a transmitter and receiver are equipped with a same random timing generator.

25 The transmitting side places pilot symbols at a random timing, which is neither cyclic nor burst-like. That is, the transmitting side creates and sends a transmission signal with pilot signals randomly distributed on a pilot channel.

In this case, other data (control information, etc.) is inserted into areas of the transmission signal where no pilot data exists.

For example, in the pilot channel shown in FIG.15, pilot signals (PL) are irregularly distributed and control data is inserted in other areas.

Hereinafter, the transmitter and receiver will be explained using FIG.9 and FIG.10. FIG.9 is a block diagram showing a configuration of the transmitter and FIG.10 is a block diagram showing a configuration of the receiver.

The transmitter in FIG.9 is equipped with random timing generation circuit 401, transmission control circuit 402, spreading circuit 403, D/A converter 404, mixer 406, carrier generation circuit 405, amplification circuit 407, band restriction circuit 408 and antenna 409.

Pilot signal spreading timings in spreading circuit 403 are controlled based on a control signal generated from random timing generation circuit 401.

On the other hand, the receiver in FIG.10 is equipped with antenna 410, band restriction circuit 411, amplification circuit 412, carrier generation circuit 413, mixer 414, A/D converter 415, random timing generation circuit 416, reception control circuit 417, despreding circuit 418 and phase/signal intensity detection circuit 419.

Random timing generation circuit 416 generates a

timing control signal under the same condition as that of the transmitter. Pilot signal desreading timings in desreading circuit 418 are controlled according to this timing control signal.

5           Thus, distributing pilot signals irregularly makes the system less susceptible to cyclic fading or burst-like fading. On the other hand, since the receiving side knows the locations of pilot signals beforehand, there is no problem with reception of pilot  
10 signals.

Furthermore, distributing pilot signals using a common random timing generator for the transmitting side and receiving side also provides a kind of encryption effect.

15           FIG.11 is a block diagram showing a specific example of an internal configuration of desreading circuit 418 shown in FIG.10.

As shown in the figure, two systems of QPSK-modulated signal (I signal and Q signal) are input to  
20 desreading circuit 418.

Desreading circuit 418 is equipped with multipliers 501a to 501d, comparators 502a and 502b, integrators 503a and 503b, code generators 505, 506, 508 and 509 and switches 507 and 510.

25           The reception timing control circuits (416 and 417) control an integration period (period for calculating correlation value) in integrators 503a and 503b. Moreover, switches 507 and 510 are switched by the

reception timing control circuits (416 and 417).

As described above, the present invention has been explained using 5 embodiments, but the present invention is not limited to these embodiments and can be modified or applied in various manners.

For example, the above embodiment changes despreding timings irregularly, but the present invention is not limited to this. That is, it is also possible to continuously despread pilot signals, temporarily store the despreding results in a buffer and randomly or adaptively select which of the stored demodulated signals should be used (picked up). In this case, though memory to temporarily store pilot signals is necessary, similar effects can be obtained.

As described above, the present invention can secure reception of always-optimal pilot signals less susceptible to fading when pilot signals are received.

The present invention can be easily implemented by simply adding the reception timing determining means to the circuit of the reception apparatus.

The explanations above describe cases of CDMA communications, but the present invention can also be applied to TDMA-based or FDMA-based communications. That is, in the case of a TDMA-based communication, it is possible to adopt a communication format in which pilot signals are randomly distributed. In the case of a FDMA-based communication, the present invention is made applicable by providing a dedicated pilot signal



channel.

The present invention is not limited to the above described embodiments, and various variations and modifications may be possible without departing from the  
5 scope of the present invention.

This application is based on the Japanese Patent Application No.2000-035052 filed on February 14, 2000, entire content of which is expressly incorporated by reference herein.